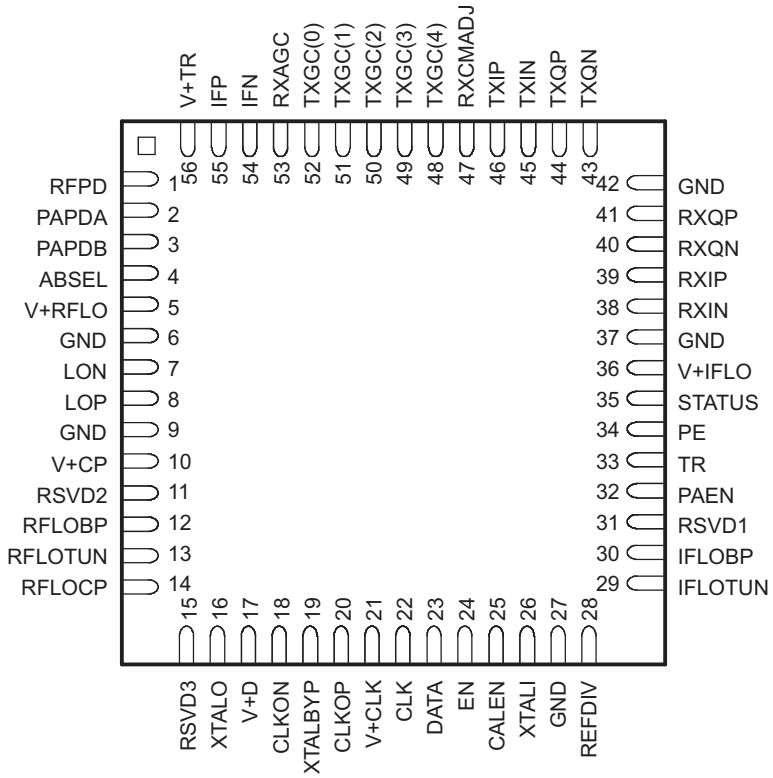
Dual-Band IQ/IF TRANSCEIVER WITH DUAL VCO SYNTHESIZERS

FEATURES

- **Highly Integrated 802.16 d/e Radio IQ/IF Transceiver PLL ASIC**
- **Fully Integrated IF and RF VCOs and Synthesizers**
- **Super Heterodyne Architecture for Superior Performance**
- **Internal PLL Reference Oscillator with Clock Output for Base-Band ASICs**
- **Internal AGC and Power Control Function**
- **IQ DC Offset Calibration Function and Anti-Aliasing Filters Integrated**
- **Differential LO and IF Interface for Enhanced Spurious Immunity**
- **RF LO Frequency Range:**
  - **2536 – 3160 MHz**
- **Phase Noise 0.5 Degrees RMS Typical Over Channel BW**
- **Reference Frequency: 40 or 44 MHz**
- **Single 3.3-V Power Supply**
- **IF = 374 MHz (Both Bands)**

RTQ PACKAGE
(TOP VIEW)



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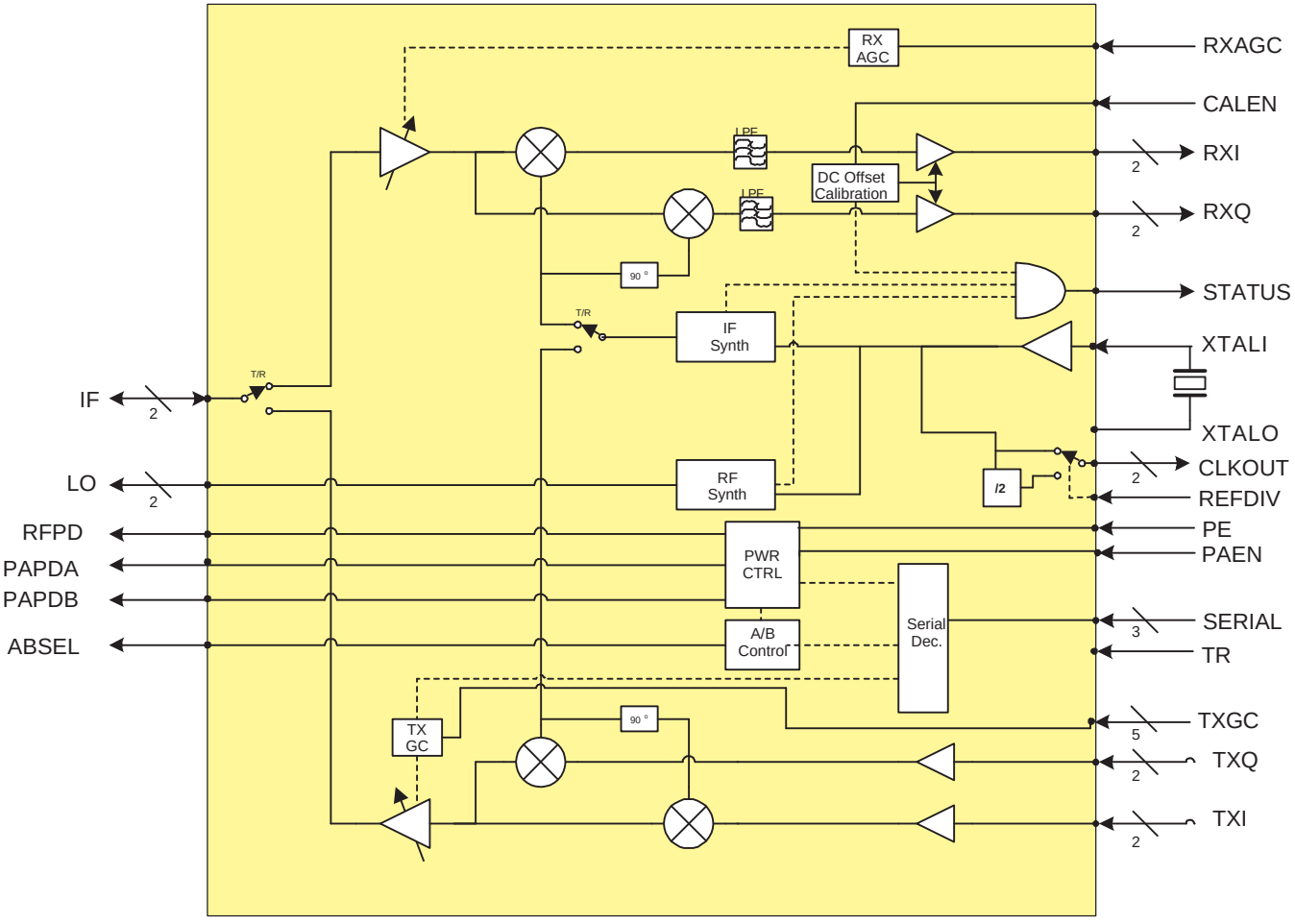
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The TRF2432 is a fully integrated IQ transceiver specifically for use in 802.16 d/e applications. The TRF2432 is designed to perform the IQ conversion at 374MHz IF as well as provide an RFLO and control logic to a TI RFFE (Radio Frequency Front End). The TRF2432 uses a common IF frequency for both bands, which eliminates the need for an additional IF filter in dual band applications. The TRF2432 has an internal IQ DC offset calibration function for the receive IQ interface. Combined with a TI integrated RFFE, the TRF2432 completes the TI WLAN two-chip radio.

The TRF2432 incorporates all of the system blocks from the modem to the RFFE except for the IF filtering and the reference crystal. The ASIC uniquely incorporates an internal PLL reference oscillator where only a crystal is needed, and also provides a clock output for base-band/MAC ASICs. TRF2432 includes two synthesizers with VCOs, IQ modulator, IQ demodulator, anti aliasing filters, IF amplifiers, receive AGC circuit, transmit power control and serial interface.

Functional Block Diagram



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DEVICE INFORMATION

Table 1. TERMINAL FUNCTIONS

TERMINAL		I/O	TYPE	DESCRIPTION
NAME	NO.			
RFPD	1	O	Analog	RFFE sleep output
PAPDA	2	O	Analog	PA band A select to RFFE
PAPDB	3	O	Analog	PA band B select to RFFE
ABSEL	4	O	Analog	A or B band select to RFFE
V+RFLO	5	I	Power	+3.3V Power Supply. RF VCO bias
GND	6	I	Analog	Connect to ground per suggested layout for normal operation
LON	7	O	RF Dif.	Positive going LO output
LOP	8	O	RF Dif.	Negative going LO output
GND	9	I	Analog	Connect to ground per suggested layout for normal operation
V+CP	10	I	Power	+3.3V Power Supply. Synthesizer Charge Pumps bias
RSVD2	11	-	-	Reserved. Leave open
RFLOBP	12	O	Analog	Bypass Capacitor for LO1 (RF)
RFLOTUN	13	I	Analog	VCO Synthesizer 1 (RF) Tuning port
RFLOCP	14	O	Analog	Synthesizer 1 (RF) Charge pump output
RSVD3	15	-	-	Reserved. Leave open
XTALO	16	I/O	Analog	Negative crystal connection
V+D	17	I	Power	+3.3V Power Supply. Digital Bias
CLKON	18	O	Digital	Negative going reference clock output (40,44,20 or 22MHz)
XTALBYP	19	O	Analog	Bypass Capacitor for crystal oscillator
CLKOP	20	O	Digital	Positive going reference clock output (40,44,20 or 22MHz)
V+CLK	21	I	Power	+3.3V Power Supply. Reference Clock Bias
CLK	22	I	Digital	Clock line of 3-wire serial bus
DATA	23	I	Digital	Data line of 3-wire serial bus
EN	24	I	Digital	Load enable line of 3-wire serial bus
CALEN	25	I	Digital	A transition high in RX active mode initiates DC offset calibration. Low disables calibration circuit. Internal pull down
XTALI	26	I/O	Analog	Positive crystal connection. Also input for external XO reference
GND	27	I	Analog	Connect to ground per suggested layout for normal operation
REFDIV	28	I	Digital	Sets reference clock divider. Set HIGH to activate divide by 2. Internal pull down.
IFLOTUN	29	I	Analog	VCO Synthesizer 2 (IF) Tune port. CP2 Connected internally
IFLOBP	30	O	Analog	Bypass Capacitor for LO2 (IF)
RSVD1	31	-	-	Reserved. Leave open.
PAEN	32	I	Digital	PA enable. HIGH enables RFFE PA. Enables PAPDA or PAPDB. Internal pull down.
TR	33	I	Digital	Transmit or Receive control line. TX=HIGH, RX=LOW. Internal pull down.
PE	34	I	Digital	Power enable. HIGH is enabled. Not defined internally.
STATUS	35	O	Digital	RF, IF and REF synthesizer lock detect and calibration status.
V+IFLO	36	I	Power	+3.3V Power Supply. IF VCO bias
GND	37	I	Analog	Connect to ground per suggested layout for normal operation
RXIN	38	O	Analog	Receiver in-phase negative going output.
RXIP	39	O	Analog	Receiver in-phase positive going output.
RXQN	40	O	Analog	Receiver quadrature negative going output.
RXQP	41	O	Analog	Receiver quadrature positive going output.
GND	42	I	Analog	Connect to ground per suggested layout for normal operation
TXQN	43	I	Analog	Transmitter quadrature negative going output.

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Table 1. TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	TYPE	DESCRIPTION
NAME	NO.			
TXQP	44	I	Analog	Transmitter quadrature positive going output.
TXIN	45	I	Analog	Transmitter in-phase negative going output.
TXIP	46	I	Analog	Transmitter in-phase positive going output.
RXCMADJ	47	I	Analog	Connect resistor to ground to adjust common mode output voltage
TXGC[4]	48	I	Digital	TX Gain Control bit 4 (MSB). Logic LOW induces 16dB Atten. Internal pull down.
TXGC[3]	49	I	Digital	TX Gain Control bit 3. Logic LOW induces 8dB Atten. Internal pull down.
TXGC[2]	50	I	Digital	TX Gain Control bit 2. Logic LOW induces 4dB Atten. Internal pull down.
TXGC[1]	51	I	Digital	TX Gain Control bit 1. Logic LOW induces 2dB Atten. Internal pull down.
TXGC[0]	52	I	Digital	TX Gain Control bit 0 (LSB). logic LOW induces 1dB Atten. Internal pull down.
RXAGC	53	I	Analog	Receiver automatic gain control pin.
IFN	54	I/O	RF Dif.	IF positive going input or output.
IFP	55	I/O	RF Dif.	IF negative going input or output.
V+TR	56	I	Power	+3.3V Power Supply. TX and RX IF amplifier bias.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		UNIT
DC supply voltage, V_{CC}		0 to 5.5 V
DC supply current, I_{CC}		600 mA
RF input power	Any port and any mode	10 dBm
Digital input voltage, V_{ID}		-0.3 V to V_{CC}+0.3 V
Analog input voltage, V_{IA}		0 to 3.6 V
Junction temperature, T_{JC}		125°C
Thermal resistance junction-to-case, θ_{JC}		25°C/W
Operating temperature, T_A		-20°C to 85°C
Storage temperature, T_{stg}		-40°C to 105°C
Lead temperature	40 sec maximum	220°C

DC CHARACTERISTICS

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	Specification compliant		2.7	3.3	3.6	V
	Transmit Mode Supply Current	TR = High, Active mode			100	125	mA
	Receive Mode Supply Current	TR = Low, Active mode			90	110	mA
	Idle Mode Supply Current				70	85	mA
	Standby Mode Supply Current				10	15	mA
	Sleep Mode Supply Current					10	µA
	DC current, V+RFLO	V_{CC} = 3.3 V, 0 < V+RFLO < V+TR + 0.6V	Standby		0		
			Idle		0		
			Tx		11		
			Rx		11		
	DC current, V+CP	V+TR - 0.6V < V+CP < V+TR + 0.6V	Standby		0		
			Idle		0.6		
			Tx		0.6		
			Rx		0.6		

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DC CHARACTERISTICS (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	DC current, V+D	V+TR - 0.6V < V+D < V+TR + 0.6V	Standby		8.5		
			Idle		50/30		
			Tx		50/30		
			Rx		50/30		
	DC current, V+CLK	V+TR - 0.6V < V+CLK < V+TR + 0.6V	Standby		4		
			Idle		4		
			Tx		4		
			Rx		4		
	DC current, V+IFLO	0 < V+IFLO < V+TR + 0.6V	Standby		0		
			Idle		0		
			Tx		8.5		
			Rx		8.5		
	DC current, V+TR	3.6 V max	Standby		0.35		
			Idle		0.35		
			Tx		33/21		
			Rx		20		

RECEIVER CHARACTERISTICS

T_A = 25°C and V_{CC} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{IF}	IF input frequency			374		MHz
	Voltage gain	Gain control < 0.3 V	62	71		dB
	Analog Gain Control Range	V_{AGC} from .3 to 2.2V	55			dB
	Gain Control Sensitivity	Monotonic.		-40	-50	dB/V
	Gain Control Linearity	From linear		±3		
	Gain settling time	Full range to within 0.5dB final gain setting		0.25		µs
	Output P_{-1dB}		-7			dBm
	Output 3rd order intercept point			4.8		Vppd
	Noise figure	From Full Gain to 40dB gain. Not to increase more than 1dB per 1dB of gain change thereafter.		7		dB
	IQ differential impedance	I, Q outputs (0-11MHz)			100	Ω
	Output load impedance	Single ended	2||10			kΩ||pF
	Output swing				1000	mVpd
	Input return loss	Measured into 200-Ω differential	9			dB
	Output common mode voltage	Adjustable by one resistor to ground. V_{com} = 0.56 + 0.48 × R_{ADJ}, R_{ADJ} is kΩ	0.6		1.4	V
	I/Q gain mismatch	0 to 11 MHz band		0.1	0.5	dB
	I/Q phase imbalance	0 to 11 MHz band		0.9	3	°
	I/Q differential DC offset	After calibration. Min Gain			10	mV
		Before calibration			50	mV
	DC offset calibration time	With 40 MHz reference. See calibration instructions		32		µs
	LPF attenuation	25 MHz	20	25		dB
		10.55 MHz		1		dB

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TRANSMITTER CHARACTERISTICS

TR = High, 2dB base band filter loss in RX band, MIN, TYP, and MAX rating are at 25°C and V_{CC} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_{ID}	Differential input impedance	I, Q inputs. (0 – 11MHz)	10			kΩ
V_{IC}	Common-mode input voltage	Effected by V+. TRF2432	1.1		2.1	V
V_I	Input voltage	I, Q inputs, differential.		0.3		Vpd
f_{IF}	IF input frequency			374		MHz
	Voltage gain	TX Gain Control Word} = {11111}(1), 200-Ω differential output	3	5		dB
	Gain control range			31		dB
	Gain step size	Per bit		1		dB
	Sideband suppression	0 to 11 MHz band	25	30		dB
	IFLO leakage	Max. gain settings. TX IQ DC offset < 1 mV		-40	-35	dBm
	Output 1dB compression	Maximum gain setting	2	4		dBm
	Output noise	Maximum Gain. Decreasing 1dB per dB attenuation until 15 dB		-137	-131	dBm/Hz
		16 to 31dB down from max gain.		-145	-144	dBm/Hz

(1) Gain is referenced to the amplitude of either the I or Q signal, when they are in quadrature. i.e. For I = 0.5 × sin (wmt) and Q = 0.5 ×cos (wmt) input in differential volts. The output at a gain of 0dB would ideally be a single tone at 0.5V differential across the 200-Ω outputs.

COMMON ELECTRICAL CHARACTERISTICS

MIN, TYP, and MAX ratings are at 25°C and V_{CC} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	IF IO differential impedance			200		Ω

SYNTHESIZER CHARACTERISTICS

RF SYNTHESIZER CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Frequency range		2536		3150	MHz
	Tuning step			250		kHz
	Settling time	±10kHz of final frequency. From Standby to Idle measured from enable		60		µs
	Phase noise (VCO)	4.5 MHz offset		-130		dBc/Hz
		20 MHz offset		-143		dBc/Hz
	Integrated phase error	10 kHz to 10 MHz		0.6		°rms
	Spurious suppression	0.25 < Δf < 3 MHz offset		-45-7Δf		dBc
		> 3 MHz offset		-70		dBc
	Power output	Into 100 Ω differential. With matching	-2	0		dBm

INTEGER MODE IF SYNTHESIZER CHARACTERISTICS

f_{REF} = 44 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Frequency	With 44 MHz crystal		374		MHz
	Settling time	±10kHz of final frequency. From Standby to Idle measured from enable		60		µs
	Integrated phase error	10 kHz to 10 MHz		0.2		°rms

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INTEGER MODE IF SYNTHESIZER CHARACTERISTICS (continued)

f_{REF} = 44 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Spurious suppression	> 3 MHz offset		-70		dBc

FRACTIONAL MODE IF SYNTHESIZER CHARACTERISTICS

f_{REF} = 40 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Frequency	With 44 MHz crystal		374		MHz
	Settling time	±10kHz of final frequency. From Standby to Idle measured from enable		60		µs
	Integrated phase error	10 kHz to 10 MHz		0.1		°rms
	Spurious suppression	0.25 < Δf < 3 MHz offset		-45-7Δf		dBc
		> 3 MHz offset		-70		dBc

PLL REFERENCE/CLOCK OUTPUT CHARACTERISTICS

The TRF2432 synthesizers operate from a single 40 or 44 MHz reference. The TRF2432 can generate its own PLL reference using an internal oscillator or it may also be driven from an external reference. The TRF2432 provides a user selectable, buffered clock output for base-band ASICs.

PLL REFERENCE OSCILLATOR SPECIFICATIONS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{REF}	Reference frequency			40 or 44		MHz
	Start-up time	From power on. Depends on Crystal characteristics		0.5		ms
	Degradation to Crystal Reference Accuracy	From crystal series resonance.		0.25		PPM
	Jitter			5	10	ps
	External XO drive	Square-wave, must be AC Coupled	0.8	1	2	V_{pp}
	Equivalent input load	Single ended		500||10		Ω||pF

RECOMMENDED CRYSTAL SPECIFICATIONS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f	Frequency	Series resonant, fundamental or 3rd overtone		40 or 44		MHz
ESR	Effective series resistance				100	Ω
C	Shunt capacitance				20	pF
	Maximum power handling				50	µW
	Frequency accuracy	Over Temperature and Process			20	PPM

CLOCK OUTPUT CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLK}	Clock output frequency	REFDIV = 1		$f_{REF}/2$		MHz
		REFDIV = 0		f_{REF}		MHz
	Output voltage swing	Differential	0.4	1		V_{ppd}
DC	Duty cycle			50%		
t_r	Rise time				3	ns

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CLOCK OUTPUT CHARACTERISTICS (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_f	Fall time				3	ns
C_L	Capacitance load	Per side			8	pF

DIGITAL INTERFACE CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		1.7			V
V_{IL}	Low-level input voltage				0.5	V
V_{OH}	High-level output voltage	100-µA load current	2			V
V_{OL}	Low-level output voltage	-100-µA load current			0.2	V

SERIAL INTERFACE TIMING REQUIREMENTS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Power Enable to Serial port on	From Sleep mode to standby mode. PE High transition.	0.5			µs
	Enable clock	Time to activate the serial port to receive clocked and data.	10			ns
	Hold time, data to clock		10			ns
	Setup time, data to clock		10			ns
	Clock low duration		10			ns
	Clock high duration		10			ns
	Setup time, clock to enable		10			ns
	Enable time	Should be held high when not programming	10			ns

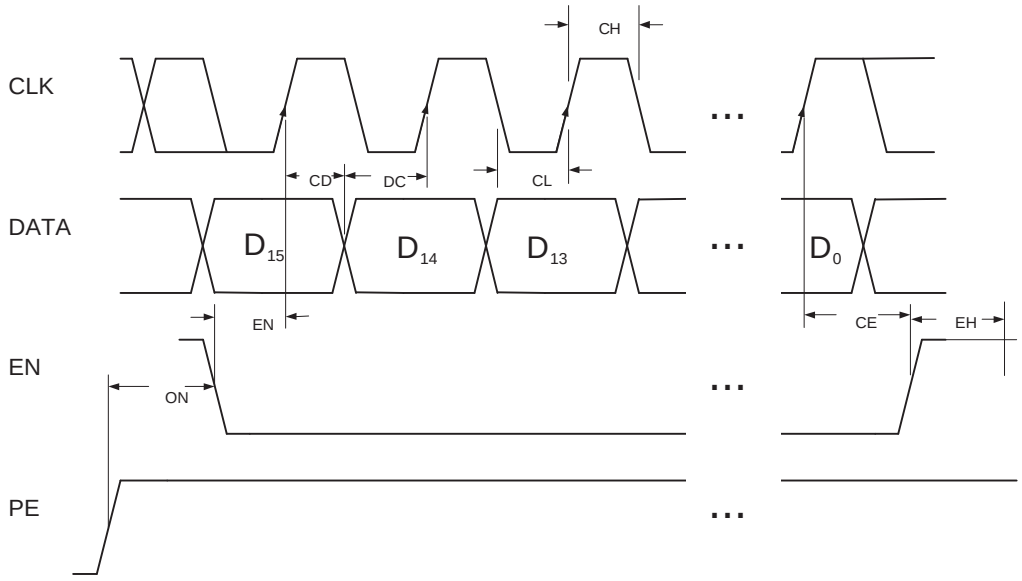


Figure 1. Serial Interface Timing Diagram

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SERIAL REGISTERS

Data is written to the registers per the following format:

Table 2. Serial Interface Data Format

REGISTERS									ADDRESS							
(MSB) 1st BIT IN																LAST BIT IN (LSB)
#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	GCX	TX_HP	REF_S	FN_IF	X	A/B	PS1	PS0	1	1	0	1	1	0	1	0
2	CP	S_INV	REF_M	GC4	GC3	GC2	GC1	GC0	1	1	0	1	1	1	1	1
3	P	MR6	MR5	MR4	MR3	MR2	MR1	MR0	1	1	0	1	1	1	0	1
4	X	FI6	FI5	FI4	FI3	FI2	FI1	FI0	1	1	0	1	1	0	0	0
5	X	MI6	MI5	MI4	MI3	MI2	MI1	MI0	1	1	0	1	1	0	0	1
6	DI4	DI3	DI2	DI1	DI0	SI2	SI1	SI0	1	1	0	1	1	0	1	1
7	XO_LP	FR6	FR5	FR4	FR3	FR2	FR1	FR0	1	1	0	1	1	1	0	0
8	DR4	DR3	DR2	DR1	DR0	SR2	SR1	SR0	1	1	0	1	1	1	1	0

Table 3. Serial Register Definitions

NAME	SYMBOL	# OF BITS	DEFAULTS(1)	DESCRIPTION
Power mode	PS	2	0	Determines mode of operation: Standby, Idle, or Active. (see Table 17)
Band A or B select	A/B	1	0	Selects TX and RX band. 1 = A band and 0 = B Band
TX gain control	GC	5	[x,x,x,x,x]	Controls gain setting of TX if CGX=0 (see below). {11111} is max gain and {00000} is minimum gain.
Spectral inversion	S_INV	1	1	Sets both the TX I/Q modulator and RX I/Q demodulator for spectral inversion. S_INV = 1 for spectral inversion. S_INV = 0 for no inversion.
Crystal pre-scalar	P	1	1	Sets the crystal or reference pre-scalar divider.
RF PLL frequency	DR	5	[0,1,0,1,0] = 10	Registers used to program the RF synthesizer operation frequency.
	SR	3	[0,0,0] = 0	
	FR	7	[0,1,1,0,0,0,0]=48	
	MR	7	[1,0,0,1,1,1,1]=79	
IF PLL frequency	DI	5	X	Registers used to program the IF synthesizer operation frequency. These registers are only effective, when the IF synthesizer is in fractional-N mode (i.e. FN_IF=1)
	SI	3	X	
	FI	7	X	
	MI	7	X	
TX gain control MUX	GCX	1	1	GCX=0 switches the Tx gain control to the serial port. GCX=1 switches the Tx gain control to the parallel input pins.
Fractional N IF synthesizer	FN_IF	1	0	FN_IF =1 enables the fractional N IF synthesizer FN = 0 sets the IF synthesizer to a fixed frequency
REF_S	REF_S	1	0	Always set REF_S = 0
REF_M	REF_M	1	0	Always set REF_M = 0
Charge Pump Current Setting	CP	1	0	CP = 1 puts charge pump for reference and fixed synthesizers into continuous current mode. CP = 0 puts synthesizers into current saving mode.
XO low power mode	XO_LP	1	1	XO_LP =1 puts crystal oscillator in low power mode. XO_LP = 0 puts the crystal oscillator full-power mode for better noise performance, and start-up time.

(1) Default values are the initial values after power up or after PE goes HIGH. “x” indicates undefined.

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Table 3. Serial Register Definitions (continued)

NAME	SYMBOL	# OF BITS	DEFAULTS(1)	DESCRIPTION
Fractional N IF synthesizer	FN_IF	1	0	FN_IF =1 enables the fractional N IF synthesizer when in idle or active mode. FN = 0 sets the IF synthesizer to a fixed frequency (374 MHz with 44 MHz crystal) for low power consumption.
TX output buffer high power	TX_HP	1	0	TX_HP = 1 puts IF amplifier in high linearity mode. TX_HP = 0 puts the IF amplifier into normal linearity mode to save current. This does not change linearity of the RFFE.

MODES OF OPERATION

Power Modes

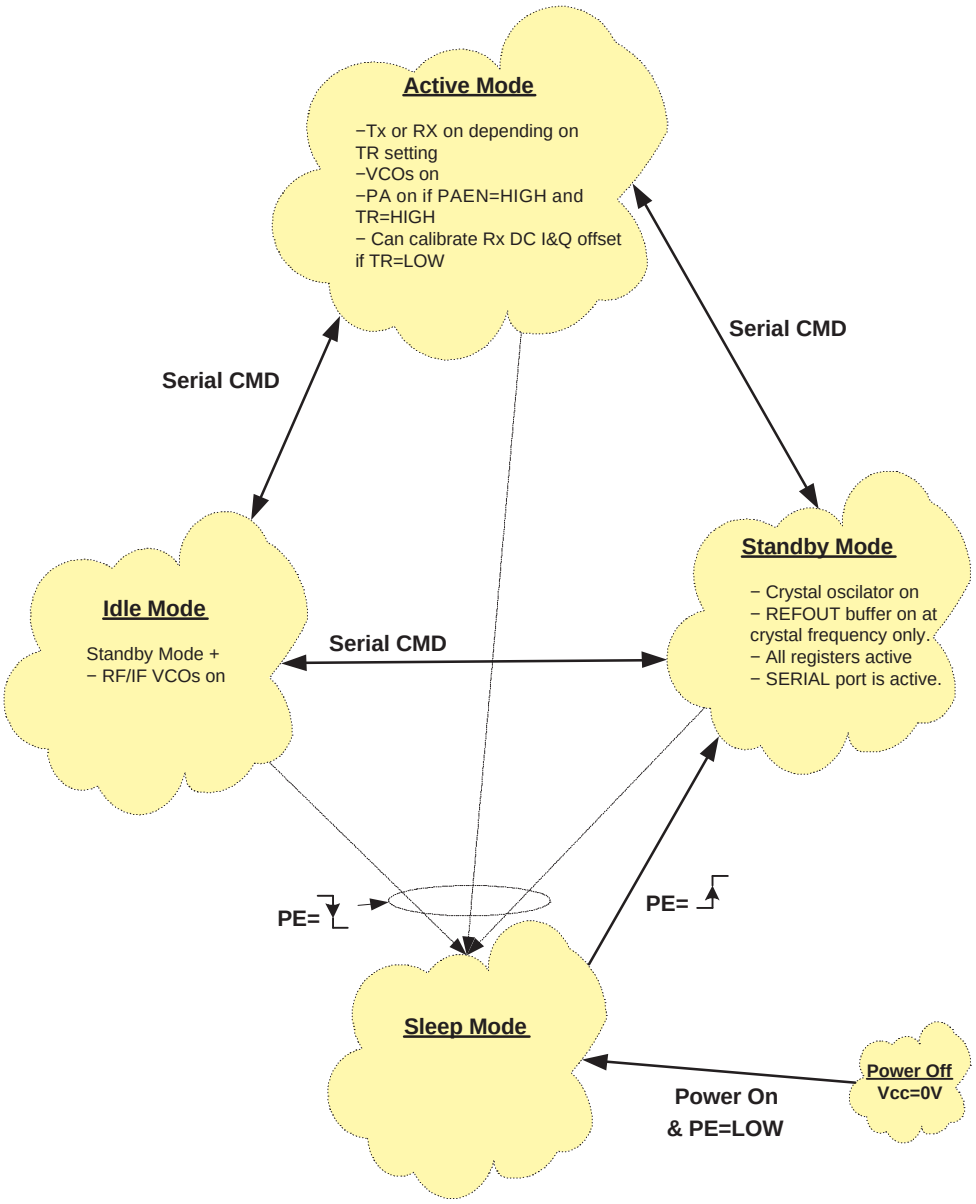


Figure 2. Power Modes

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Table 4. Power Mode Description

MODE	PS1	PS0	RFFE	TX	RX	IF PLL	RF PLL	CLK OUT	XO	SERIAL	COMMENTS
Active	1	1	X	X	X	X	X	X	X	X	TR_SEL controls Transmit/Receive mode
Idle	0	1				X	X	X	X	X	Register settings retained
Standby		0						X	X	X	Register settings retained
Sleep											Settings not required

Input/Output Modes

The TRF2432 is designed to control power and band status for a TI RFFE. The TRF2432 is designed to drive external P-MOSFETs to power up and down the appropriate sections of the RFFE. Table 4 lists the various modes of the TRF2432 and the input parameters required to enter each mode. The corresponding outputs to the RFFE are also described. Figure 4 illustrates the power control interface and recommended P-MOSFET circuit.

Table 5. Inputs/Outputs and Operational States

OPERATION STATE	INPUT PARAMETERS							OUTPUT DRIVERS				INTERNAL FUNCTIONS				
	PINS				REGISTERS											
	PE	TR	PAEN	CALEN	PS1	PS0	A/B	PAPDA	PAPDB	RFPD	ABSEL	TX	RX	SYNTHESIZERS	CRYSTAL OSC. AND DRIVER	SERIAL BUS
Sleep mode	Low	X	X	X	X	X	X	High	High	High	Low	Off	Off	Off	Off	Off
Standby mode	High	X	X	X	X	0	X	High	High	High	Low	Off	Off	Off	On	On
Idle mode	High	X	X	X	0	1	X	High	High	High	Low	Off	Off	Enabled	On	On
Active mode (PA disabled)	High	X	Low	X	1	1	X	High	High	Low	=(A/B)	Enabled	Enabled	Enabled	On	On
Active mode (RX A band)	High	Low	Low	X	1	1	1	High	High	Low	High	Off	On	Enabled	On	On
Active mode (TX A band)	High	High	High	X	1	1	1	Low	High	Low	High	On	Off	Enabled	On	On
Active mode (RX B band)	High	Low	Low	X	1	1	0	High	High	Low	Low	Off	On	Enabled	On	On
Active mode (TX B band)	High	High	High	X	1	1	0	High	Low	Low	Low	On	Off	Enabled	On	On
Active mode (RX-Cal.)	High	Low	Low	Rising Edge	1	1	X	High	High	High[1]	=(A/B)	Off	On	Enabled	On	On

(1) Held in open state until calibration is complete or disabled (CAL_EN = High -> Low).

SYNTHESIZER PROGRAMMING

The RF synthesizer frequency is programmed with four bytes: DR, SR, FR and MR and the crystal pre-scalar: P. See digital interface characteristics for programming instructions). The RF PLL locking frequency is calculated as follows:

$$f_{RFLO} = \frac{f_{RCF}}{(P + 1)} \times \left[8 \times (DR + 3) - SR - \frac{FR}{(MR + 1)} \right] \quad (1)$$

f_{REF} is the crystal reference frequency. On power-up the default register values (P=1, DR=10, SR=0, FR=48 and MR=79) with a 40-MHz crystal will attempt to lock the RFLO to 2068 MHz. The valid register ranges are listed below.

Table 6. Valid RF Register Ranges

REGISTER	MIN	MAX
DR	7	31
SR	0	7
FR	0	MR
MR	32	127

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The IF frequency synthesizer defaults to integer mode (FN_IF =0) to operate from a 44 MHz reference and is preset for 374 MHz IF. When using a 40 MHz reference, the synthesizer must be set to fractional mode (FN_IF =1) and programmed. The synthesizer is programmed with four bytes DI, SI, FI and MI. The register programming values for the IF synthesizer when using a 40 MHz reference are listed in Table 21.

Table 7. IF Register Values for 40-MHz Reference

REGISTER	VALUE
DI	16
SI	2
FI	32
MI	79

RFFE POWER CONTROL INTERFACE

The TRF2432 will control the RFFE power for all radio operational modes through three external P-MOSFETs. The suggested circuit is illustrated in Figure 4.

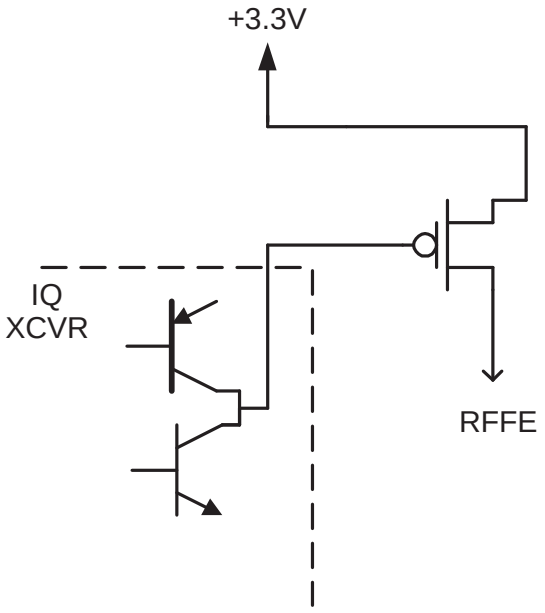


Figure 3.

IQ DC Calibration

The TRF2432 receiver has an IQ DC offset calibration function. This operation can be performed in receiver active mode only. The calibration process is entered by a rising edge on CALEN, which remains high as long as the calibration is required. The calibration procedure is as follows:

1. Set to RX active mode
2. Wait for RF and IF Synthesizers to lock: STATUS=HIGH
3. Set Rx AGC to min gain
4. Set CALEN=HIGH to enter calibration mode:
   a. IQ Transceiver turns off RFFE
   b. Internal calibration process runs
   c. The Status bit is low during calibration procedure and returns high once the calibration is complete
5. Hold CALEN HIGH to maintain calibration
6. Return to RX active Mode

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Notes on Calibration:

1. Calibration is retained as long as CALEN=HIGH and the RF2432 is **not** put into Sleep Mode.
2. To Reset calibration, set CALEN=LOW.
3. If CALEN is held LOW then calibration circuit is completely disabled, and does not contribute to any DC offset.

IQ DC Calibration Timing

Table 8. Calibration Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Calibration reset		4			µs
	Status low				1	µs
	Calibration time	1 tick = 44/f_{REF} (e.g., f_{REF} = 44 MHz, tick = 1 µs)			68	tick

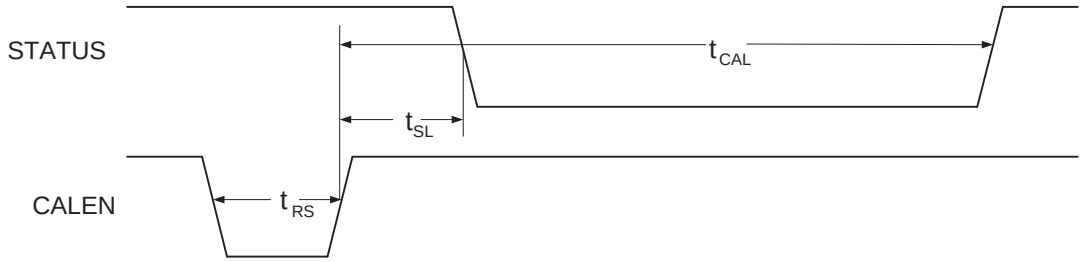


Figure 4. Calibration Timing

TYPICAL CHARACTERISTICS

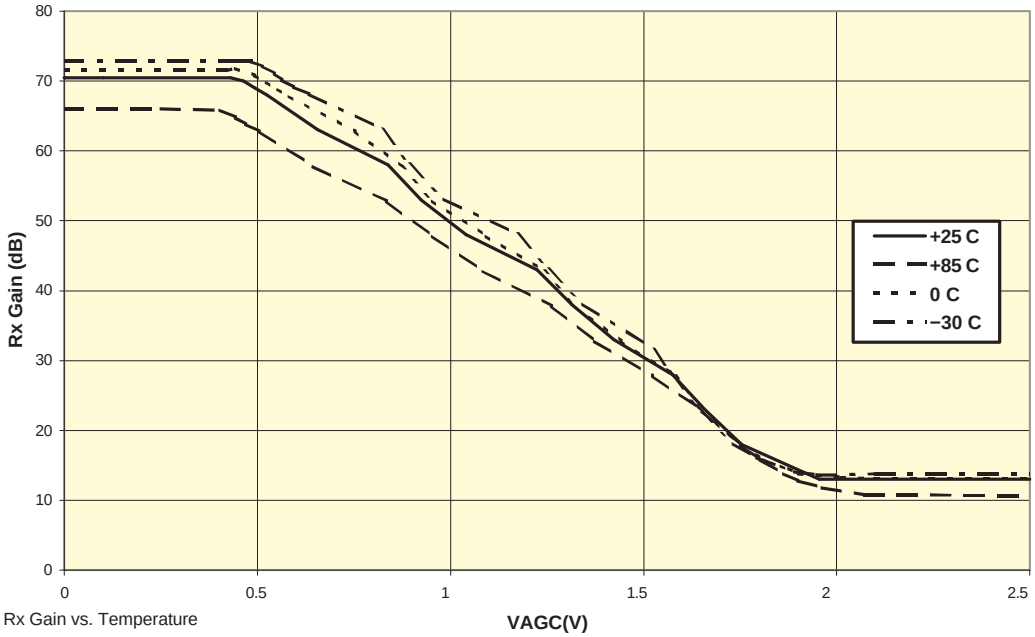
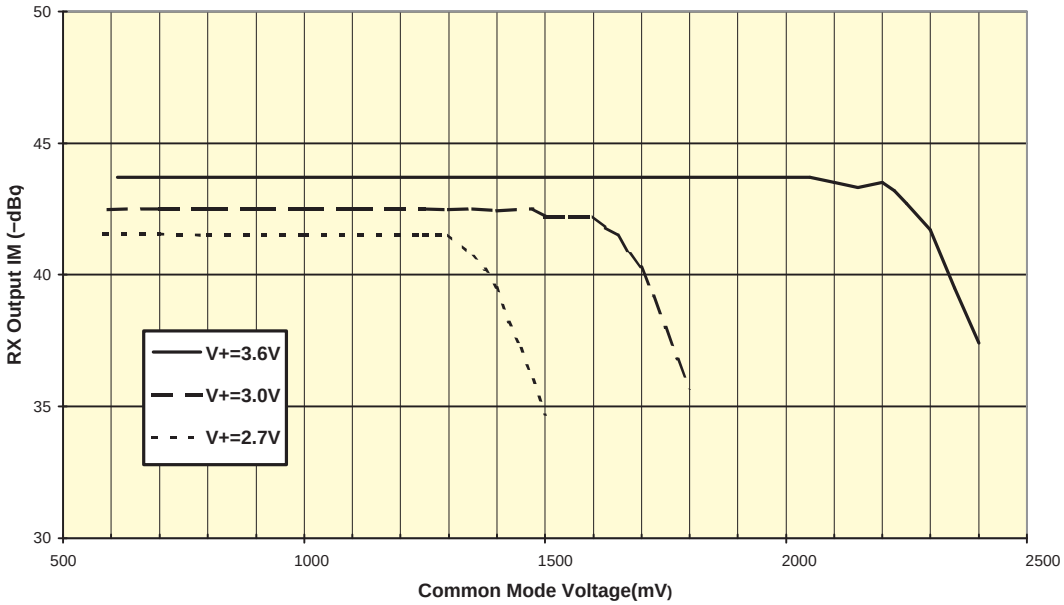


Figure 5. RX Gain Control vs Temperature

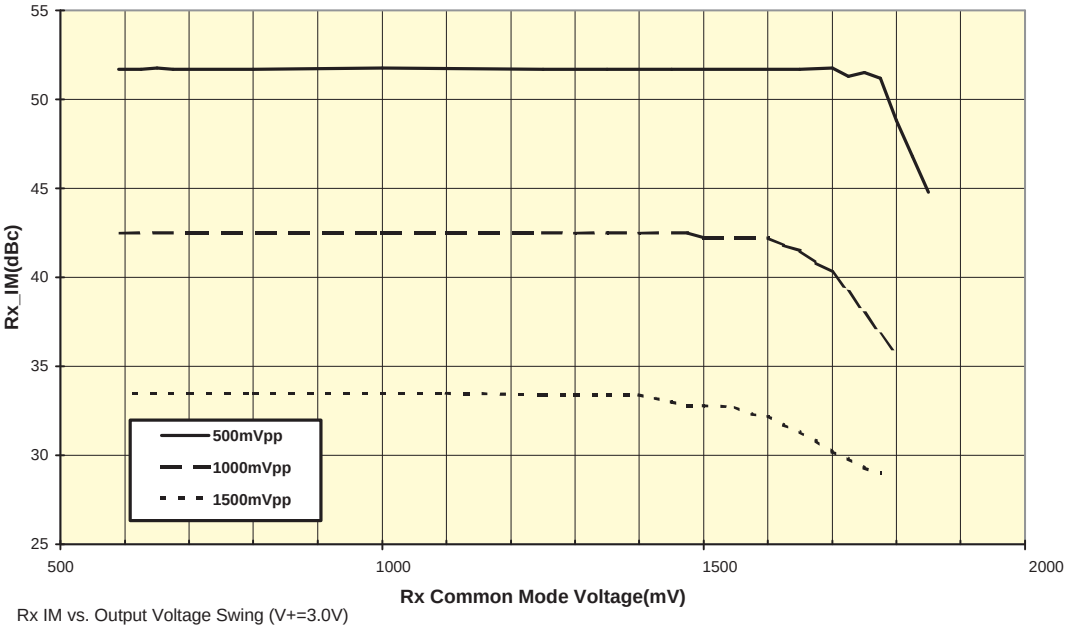
TYPICAL CHARACTERISTICS (continued)



Rx Output IM vs. Common Mode Voltage

Note: Output set for 1000 mVpp total swing. Input −40 dBm/tone.

Figure 6. RX Intermod Level vs Common-Mode Voltage



Rx IM vs. Output Voltage Swing (V+=3.0V)

Figure 7. RX Intermod. Level vs Output Voltage Swing

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TYPICAL CHARACTERISTICS (continued)

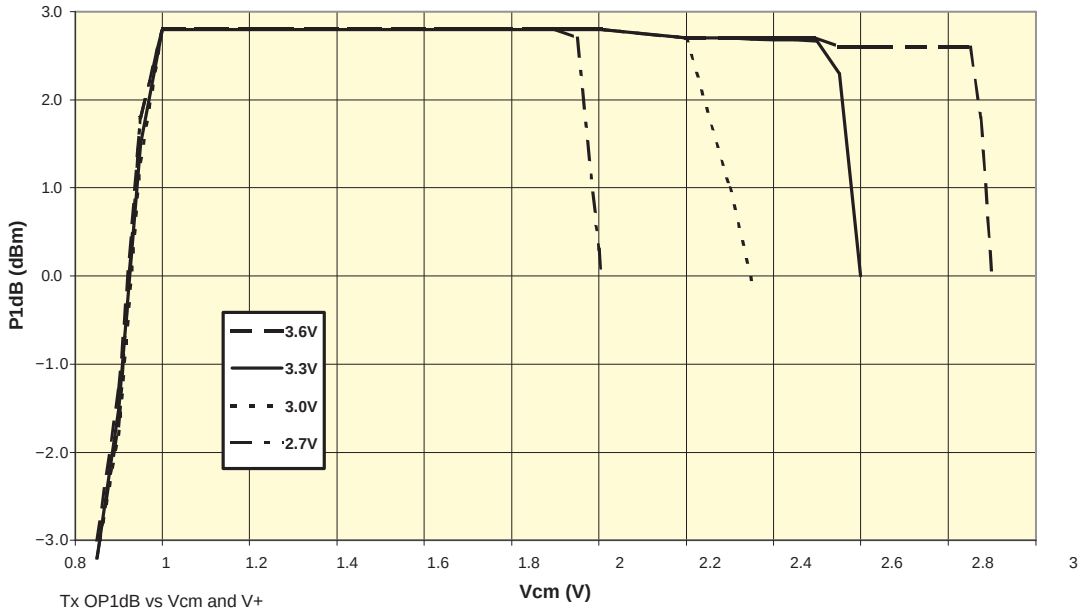


Figure 8. TX OP1dB vs Common-Mode Input Voltage

RF SYNTHESIZER PERFORMANCE

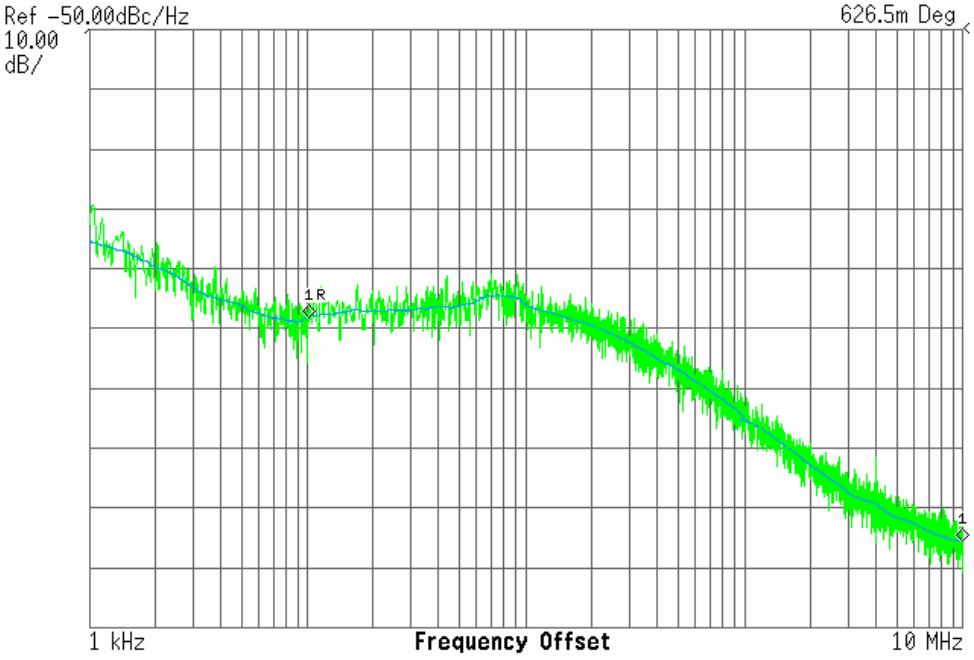


Figure 9. RFLO Phase Noise

RF SYNTHESIZER PERFORMANCE (continued)

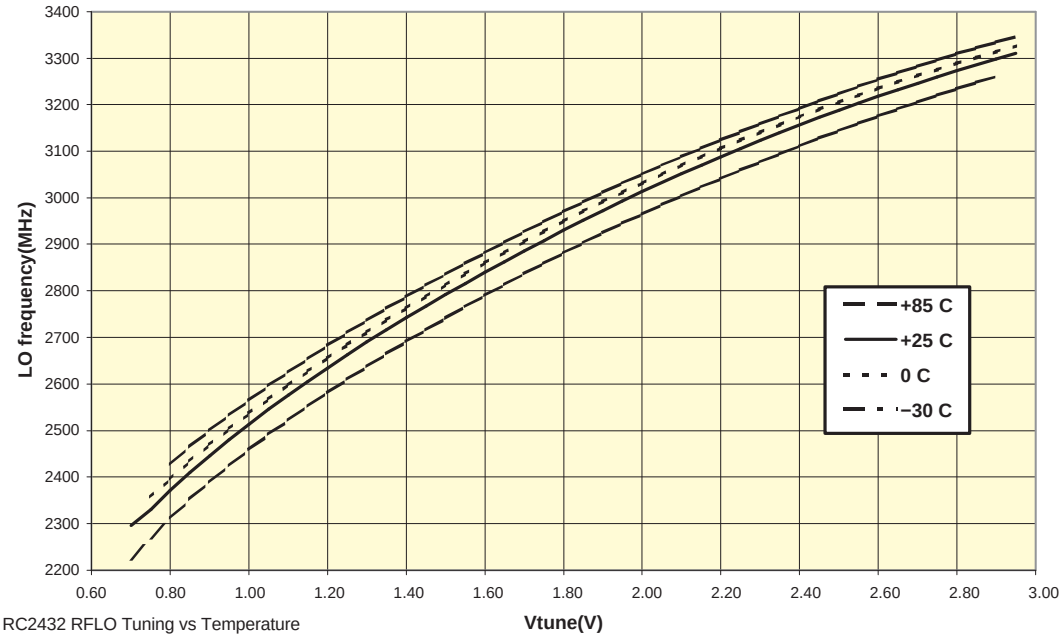


Figure 10. RF VCO Tuning Curves vs Voltages

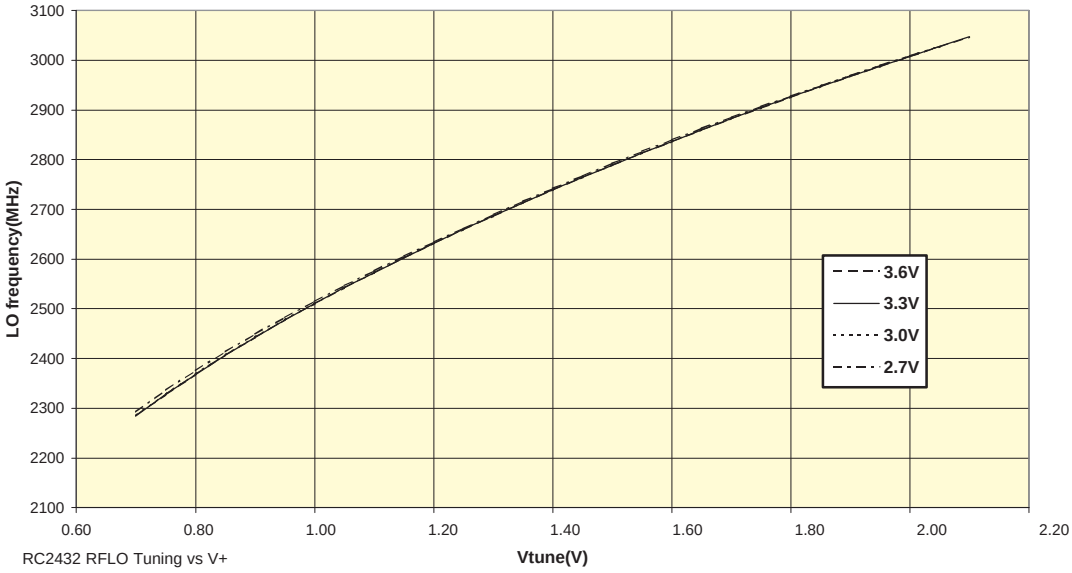


Figure 11. RF VCO Tuning Curves vs Temperature

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RF SYNTHESIZER PERFORMANCE (continued)

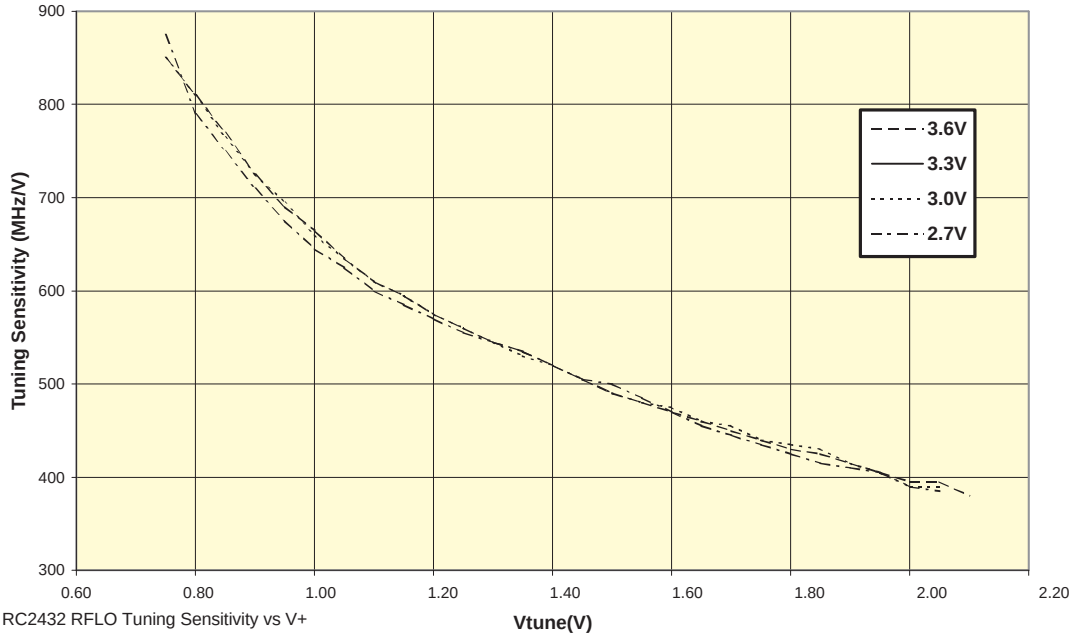


Figure 12. RF VCO Tuning Sensitivity vs V_{CC}

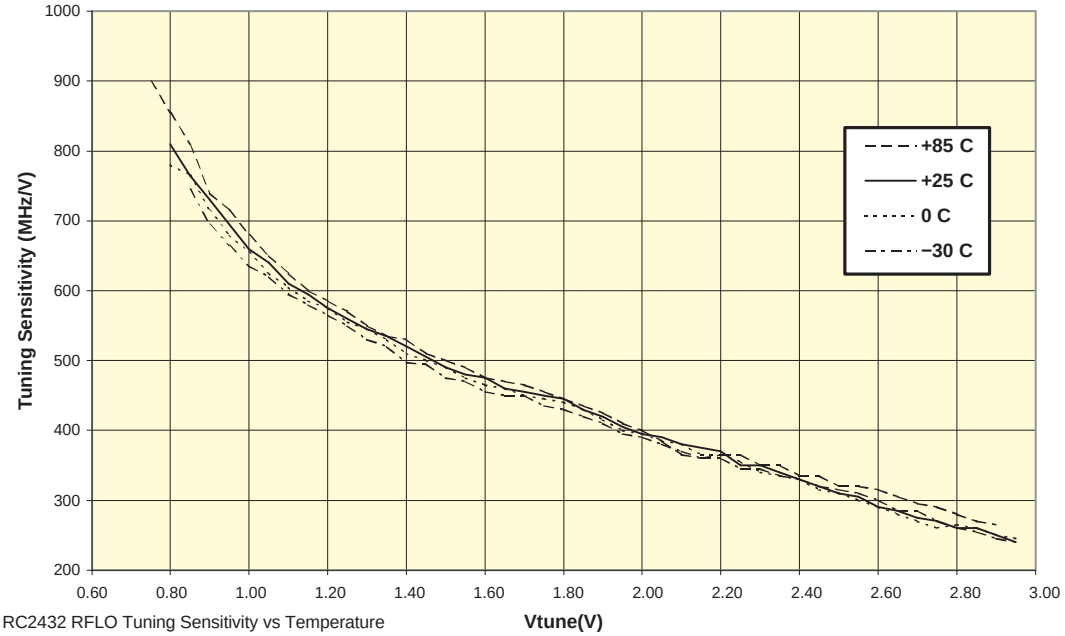


Figure 13. RFLO Tuning Sensitivity vs Temperature

IF SYNTHESIZER PERFORMANCE

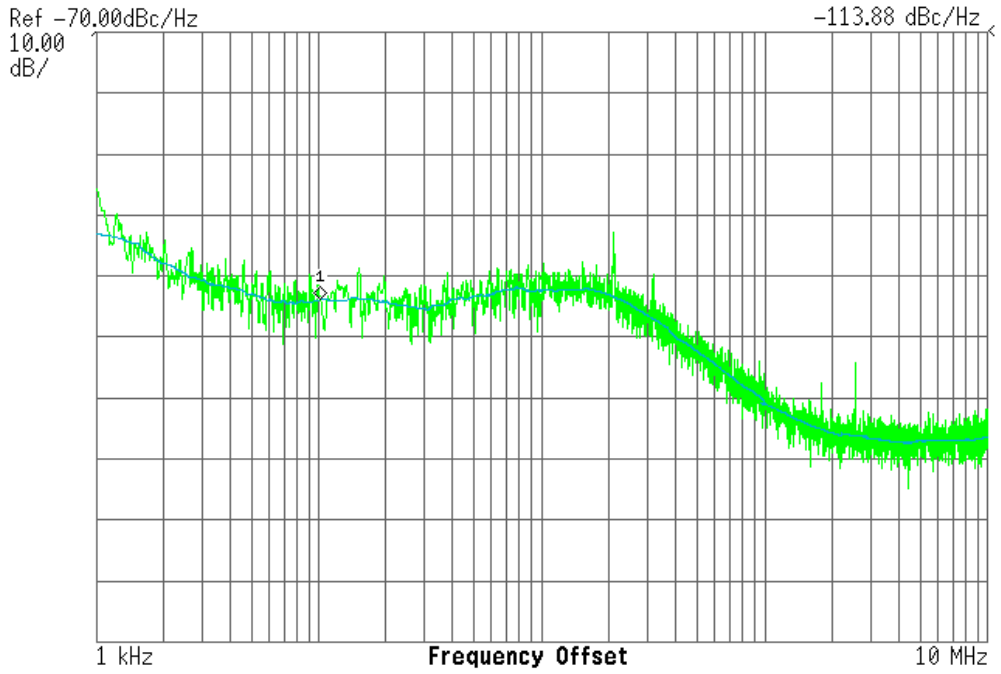


Figure 14. IF Synthesizer Phase Noise

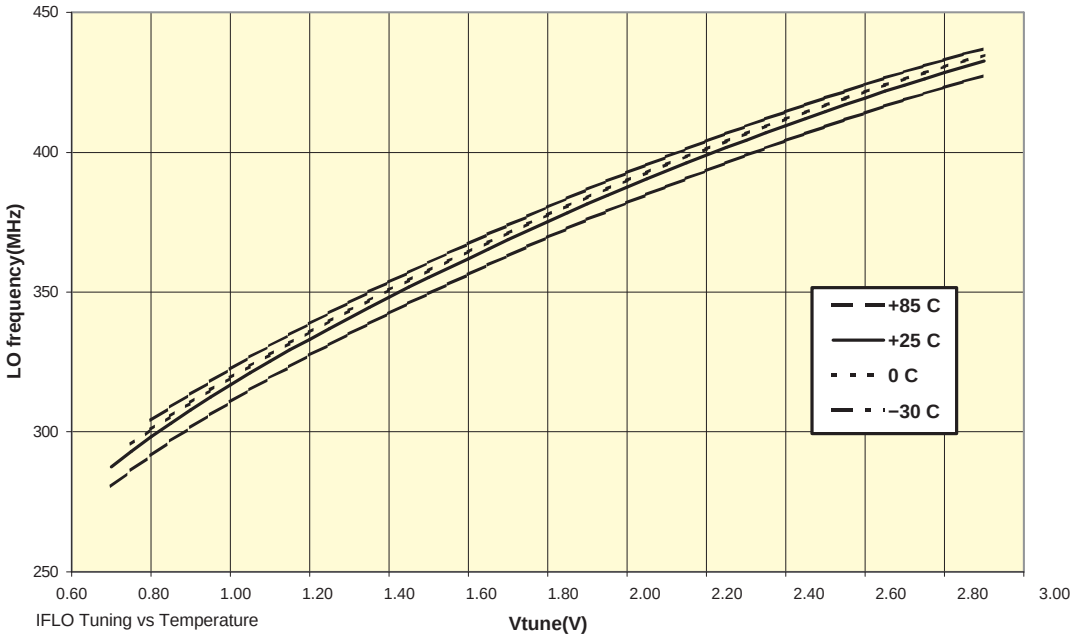


Figure 15. IFLO Tuning Curves vs Temperature

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IF SYNTHESIZER PERFORMANCE (continued)

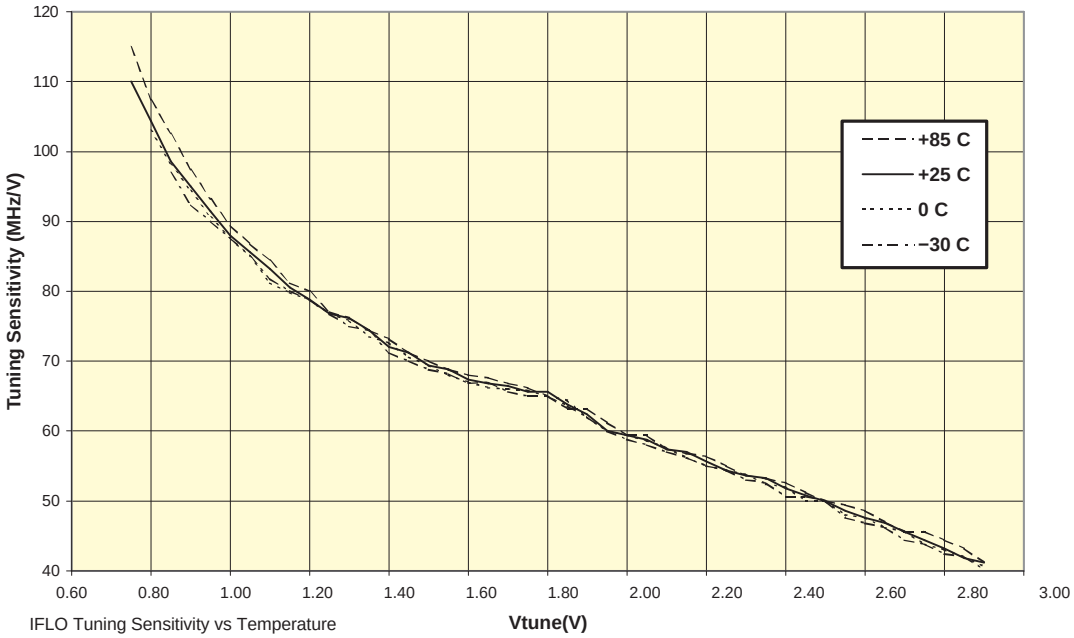


Figure 16. IFLO Tuning Sensitivity vs Temperature

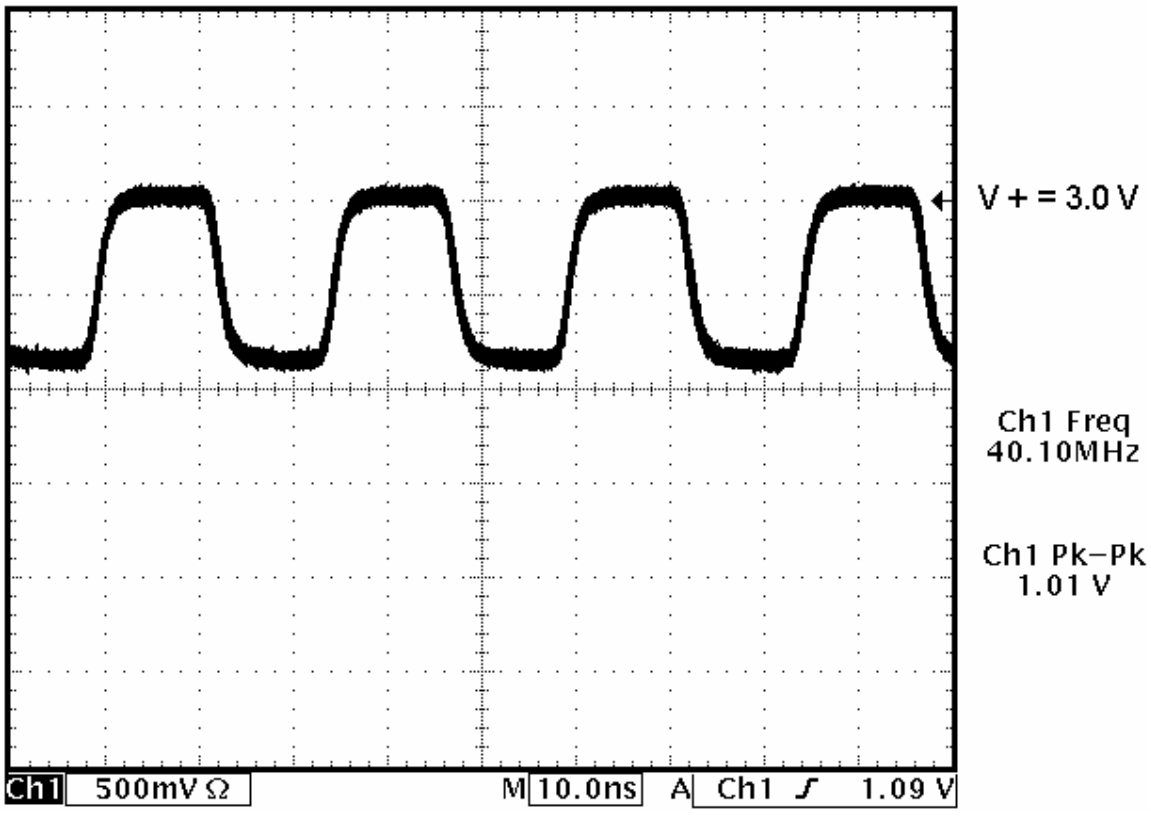


Figure 17. Reference Clock Differential Output

APPLICATION INFORMATION

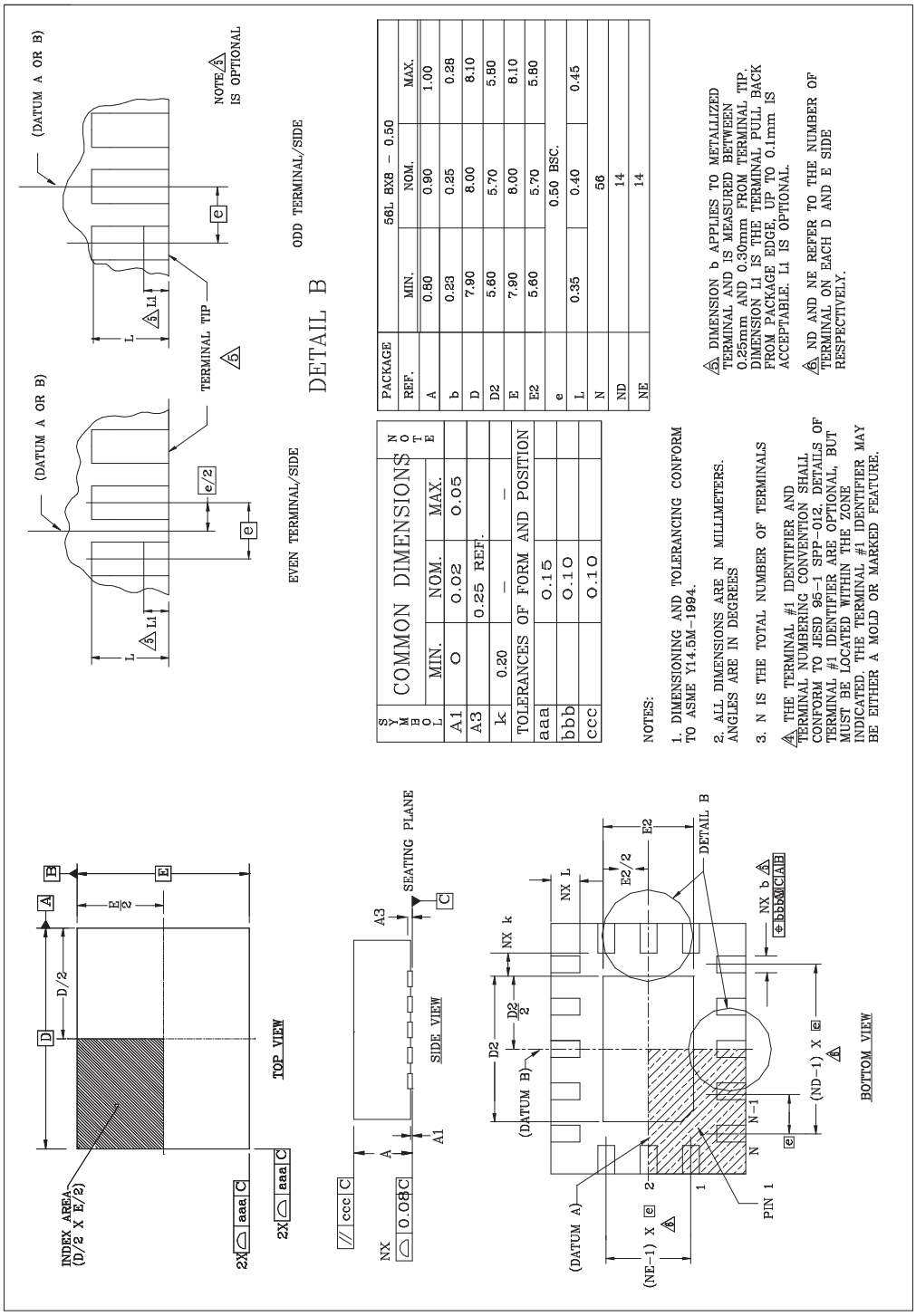


Figure 18. Package Dimensions

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF2432IRTQR	LIFEBUY	QFN	RTQ	56		TBD	Call TI	Call TI	-40 to 85	TRF 2432	
TRF2432IRTQRG3	LIFEBUY	QFN	RTQ	56		TBD	Call TI	Call TI	-40 to 85	TRF 2432	
TRF2432IRTQT	LIFEBUY	QFN	RTQ	56		TBD	Call TI	Call TI	-40 to 85	TRF 2432	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

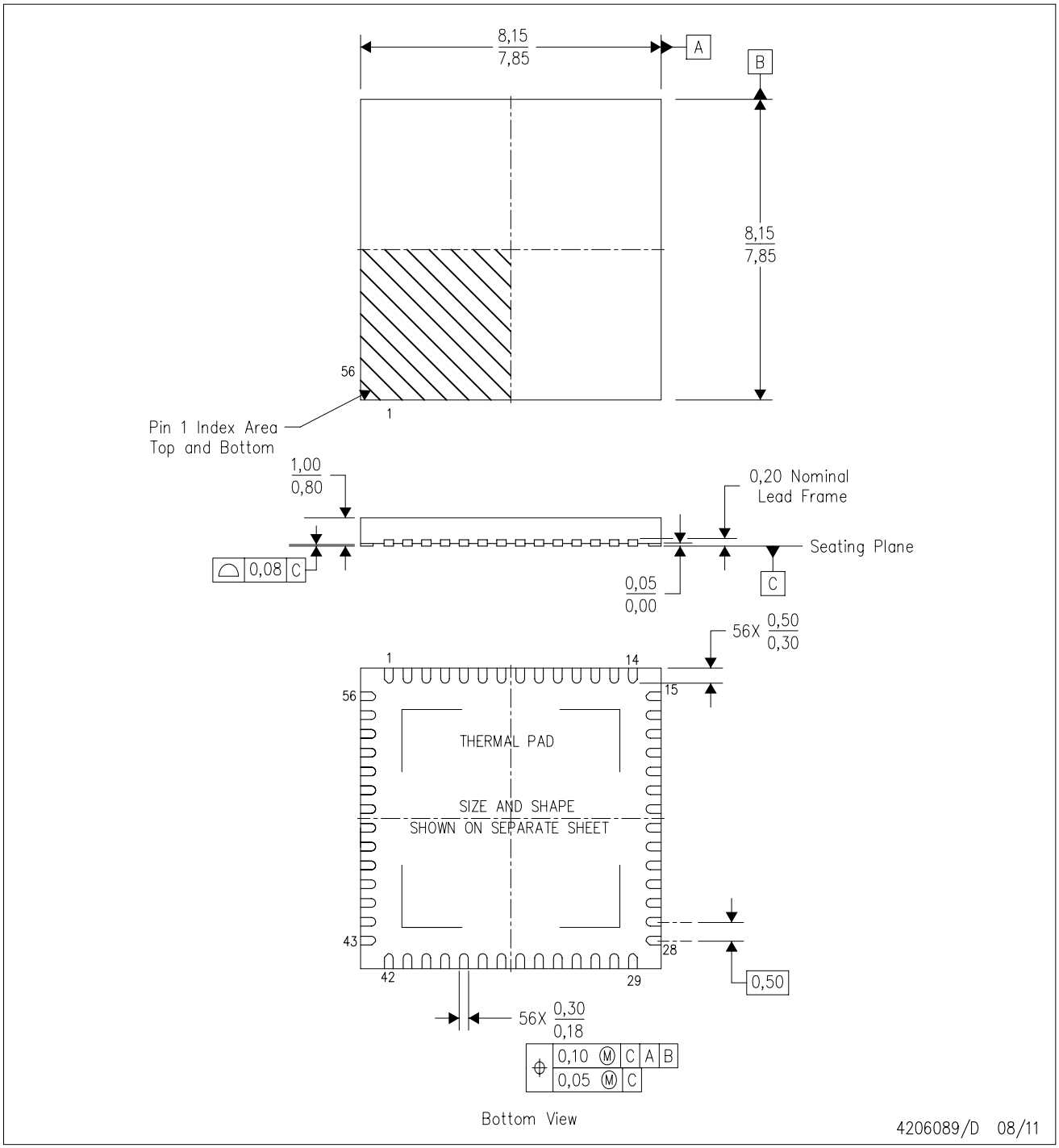
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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RTQ (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220.

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